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Attorneys for Defendants
 MATROX ELECTRONIC SYSTEMS LTD. and
 MATROX GRAPHICS INC.

UNITED STATES DISTRICT COURT
 NORTHERN DISTRICT OF CALIFORNIA
 SAN FRANCISCO DIVISION

RICOH COMPANY, LTD.,

Plaintiff,

vs.

AEROFLEX INCORPORATED, AMI
 SEMICONDUCTOR, INC., MATROX
 ELECTRONIC SYSTEMS LTD., MATROX
 GRAPHICS INC., MATROX
 INTERNATIONAL CORP., and MATROX
 TECH, INC.,

Defendants.

) Case No.
)
) **DECLARATION OF ED DWYER IN**
) **SUPPORT OF MATROX ELECTRONIC**
) **SYSTEMS, LTD. AND MATROX**
) **GRAPHICS INC.'S MOTION FOR**
) **SUMMARY JUDGMENT OF**
) **NONINFRINGEMENT**
)
) Date: December __, 2003
) Time: 9:30 a.m.
) Ctrm: 11, 19th Floor
) Hon. Martin J. Jenkins
)

I, Ed Dwyer, declare as follows:

1. I am the Vice-President of Matrox International Corporation. I have been an employee of Matrox Electronic Systems Ltd ("Matrox Electronic") from 1978 until 1994 and of Matrox Graphics Inc. ("Matrox Graphics") from 1994 until 2003, and I am familiar with the Canadian Matrox entities' operations and facilities from 1978 to the present. I make this Declaration of my personal knowledge, and if called as a witness, I could and would testify competently to the statements contained herein.

2. Engineers at Matrox Electronic and Matrox Graphics design new application specific integrated circuits (ASICs). The process of designing ASICs includes many steps. The design of the circuit includes the steps of:

- i) identification of functions to be performed by the new ASIC and preparation of design specifications identifying those functions;
- ii) design of circuitry to perform the functions described in the specification;
- iii) verification of the functionality of the circuit design;
- iv) generating the design information known as physical layout using software for placement and routing of the components and their interconnections;
- v) verification of the physical layout with the software processes used for timing characterization, design rule checking, etc.

3. Once the designs have been completed and verified, Matrox arranges with third party semiconductor fabrication companies, or foundries. These foundries perform the following steps in the process of creating ASICs:

- vi) preparation of mask data from the physical layout information to generate a set of instructions used by electron beam equipment to make photomasks (a process referred to as "fracturing");
- vii) fabrication of semiconductor wafers using the photomasks; and
- viii) dicing and verification of the resultant semiconductor circuits.

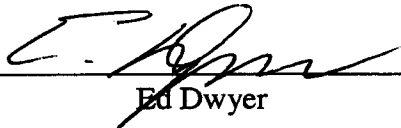
4. Typically fabrication of semiconductor wafers includes the use of up to 25 photomasks and hundreds of process steps in the manufacture of the semiconductor wafers. Matrox Electronic and Matrox Graphics have used United Microelectronics Corp. (UMC), NEC and Toshiba. The semiconductor foundries used by these companies are located either in Japan or Taiwan.

5. Design Compiler is logic synthesis software used in the design of integrated circuits. When logic synthesis software is used it makes up part of the circuit design task (step ii, above). Design Compiler is not used in the manufacturing process of either the photomasks or the chips themselves.

6. Both Matrox Electronic and Matrox Graphics are Canadian corporations with their principal places of business in Dorval, Quebec. Matrox Electronic is an industry leader in digital video production hardware and Image processing hardware and software, and Matrox Graphics is a highly acclaimed manufacturer of graphics cards for use with LCD video displays.

1 7. Matrox Electronic and Matrox Graphics are involved in the design of integrated
2 circuits, for which process they employ logic synthesis tools, such as Synopsys' Design Compiler. All
3 of the engineers and other technical personnel employed by Matrox Graphics and Matrox Electronic
4 who used those logic synthesis tools to perform design work are employed in Canada and have
5 performed, and continue to perform the entirety of the companies' design work within Canada. None
6 of these companies' design work is performed in the United States.

7 I declare under penalty of perjury under the laws of the United States of America that the
8 foregoing is true and correct. This declaration was executed in Dorval, Quebec, Canada on November
9 13, 2003.

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